7110
1 MEGABIT BUBBLE MEMORY

7110	0-50°C
7110-1	0-70°C
7110-2	10-50°C

- **1,048,576 Bits of Usable Data Storage**
- **Non-Volatile, Solid-State Memory**
- **True Binary Organization — 512 Bit Page and 2048 Pages**
- **Major Track — Minor Loop Architecture**
- **Redundant Loops with On-Chip Loop Map and Index**
- **Block Replicate for Read; Block Swap for Write**
- **Single Chip 20-Pin Dual In-Line Leadless Package and Socket**
- **Small Physical Volume**
- **Low Power per Bit**
- **Maximum Data Rate 100 Kbit/sec**

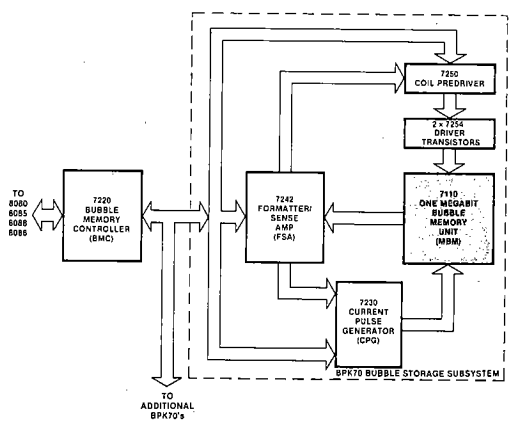
The Intel Magnetics 7110 is a very high density 1 megabit non-volatile, solid-state memory utilizing the magnetic bubble technology. The usable data storage capacity is 1,048,576 bits. The defect tolerant design incorporates redundant storage loops. The gross capacity of Intel Magnetics bubble memory is 1,310,720 bits.

The 7110 has a true binary organization to simplify system design, interfacing, and system software. The device is organized as 256 data storage loops each having 4096 storage bits. When used with Intel Magnetics complete family of support electronics the resultant minimum system is configured as 128K bytes of usable data storage. The support circuits also provide automatic error correction and transparent handling of redundant loops.

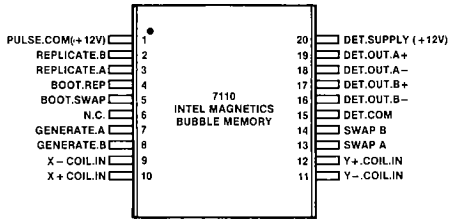
The 7110 has a major track-minor loop architecture. It has separate read and write tracks. Logically, the data is organized as a 512 bit page with a total of 2048 pages. The redundant loop information is stored on-chip in the bootstrap loop along with an index address code. When power is disconnected, the 7110 retains the data stored and the bubble memory system is restarted when power is restored via the support electronics under software control.

The 7110 is packaged in a dual in-line leadless package complete with permanent magnets and coils for the in-plane rotating field. In addition, the 7110 has a magnetic shield surrounding the bubble memory chip to protect the data from externally induced magnetic fields.

The 7110 operating data rate is 100 Kbit/sec. The 7110 can be operated asynchronously and has start/stop capability.



Block Diagram of Single Bubble Memory System — 128K Bytes



NOTE THAT PINS 13 AND 14 SHOULD BE EXTERNALLY CONNECTED.

PIN CONFIGURATION

GENERAL FUNCTIONAL DESCRIPTION

The Intel Magnetics 7110 is a 1 megabit bubble memory module organized as two identical 512K binary half sections. See Major Track-Minor Loop architecture diagram. Each half section is in turn organized as two 256K subsections referred to as *quads*.

The module consists of a bubble die mounted in a substrate that accommodates two orthogonal drive coils that surround the die. The drive coils produce a rotating magnetic field in the plane of the die when they are excited by 90° phase shifted triangular current waveforms. The rotating in-plane field is responsible for bubble propagation. One drive field rotation propagates all bubbles in the device one storage location (or cycle). The die-substrate-coil sub-assembly is enclosed in a package consisting of permanent magnets and a shield. The shield serves as a flux return path for the permanent magnets in addition to isolating the device from stray magnetic fields. The permanent magnets produce a bias field that is nearly perpendicular to the plane of the die. This field supports the existence of the bubble domains.

The package is constructed to maintain a 2.5 degree tilt between the plane of the bias magnet faces and the plane of the die. This serves to introduce a small component of the bias field into the plane of the die. During operation when the drive coils are energized this small in-plane component is negligible. During standby or when power is removed the small inplane field ensures that the bubbles will be confined to their appropriate storage locations. The direction of the in-plane field introduced by the package tilt (holding field) is coincident with the 0° phase direction of the drive field.

Quad Architecture

A 7110 quad sub-section is composed of the following elements shown on the architecture diagram.

1) Storage Loops
   Eighty identical 4096 bit storage loops provide a total maximum capacity of 327,680 bits. The excess storage is provided for two purposes: a) it allows a redundancy scheme to increase device yield; and b) it provides the extra storage required to implement error correction.

2) Replicating Generator (GEN)
   The generator operates by replicating a seed bubble that is always present at the generator site, (GEN).

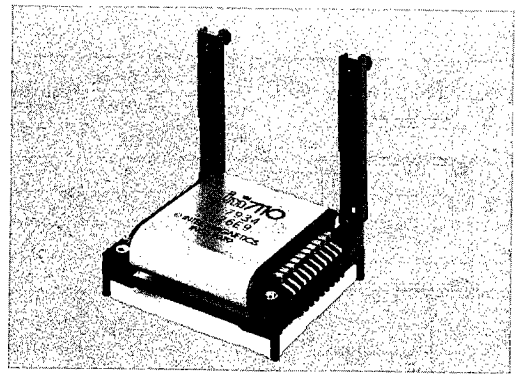
3) Input Track and Swap Gate
   Bubbles following generation are propagated down an input track. Bubbles are transferred to/from the input track from/to the 80 storage loops via series connected swap gates spaced every four propagation cycles along the track. The swap gate's ability to transfer bubbles in both directions during an operation eliminates the overhead associated with removing old data from the loops before new data can be written. The swap gate is designed to function such that the logical storage loop position occupied by the bubble transferred out of each loop is filled by the bubble being transferred into each loop. Transferred out bubbles propagate down the remaining portion of the input track where they are dumped into a bubble bucket guard rail.

4) Output Track and Replicate Gate
   Bubbles are read out of the storage loops in a non-destructive fashion via a set of replicate gates. The bubble is split in two. The leading bubble is retained in the storage loop and the trailing bubble is transferred onto the output track. Replicate gates are spaced every four propagation cycles along the output track.

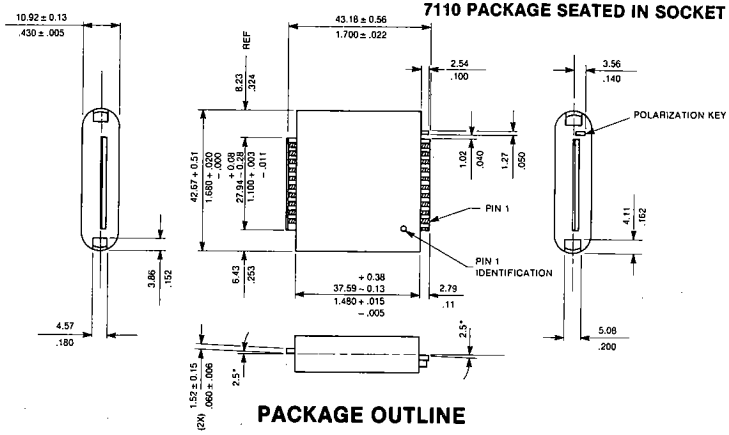
5) Detector
   Bubbles, following replication, are propagated along the output track to a detector that operates on the magneto-resistance principle. The cylindrical bubble domains are stretched into long strip domains by a chevron expander and are then propagated to the active portion of the detector. The detector consists of a stack of interconnected chevrons through which a current is passed. As the strip domain propagates through the stack, its magnetic flux causes a fractional change in stack resistance which produces an output signal on the order of a few millivolts. The strip domain following detection is propagated to a bubble bucket guard rail. A "dummy" detector stack sits in the immediate vicinity. It is connected in series with the active detector and serves to cancel common mode pickup which originates predominately from the in-plane drive field.

6) Boot Loop, Boot Swap, and Boot Replicate
   One of the two quads in each half chip contains a functionally active Boot Storage Loop. This loop is used to store:
   a) A loop mask code that defines which loops within the main storage area should be accessed. Faulty loops are "masked out" by the support electronics.
   b) A synchronization code that assigns data addresses (pages) to the data in the storage loops. Since bubbles move from one storage location to the next every field rotation, the actual physical location of a page of data is determined by the number of field rotations that have elapsed with respect to a reference.

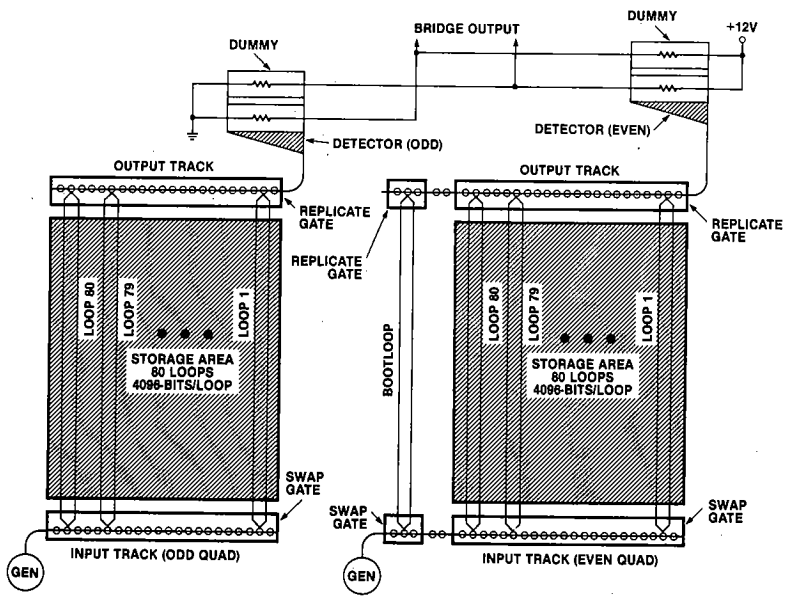
The boot loop is read from and written into via the same input and output tracks as the main storage loops. However, it has independently accessed swap and replicate gates. The boot swap, under normal circumstances, is intended only to be used during basic initialization at the factory at which time loop mask and synchronization codes are written. The boot replicate is intended to be accessed every time power is applied to the bubble module and its peripheral control electronics. At such a time, the control electronics would read and store the mask information, plus utilize the synchronization information to establish the location of the data circulating within the loops.



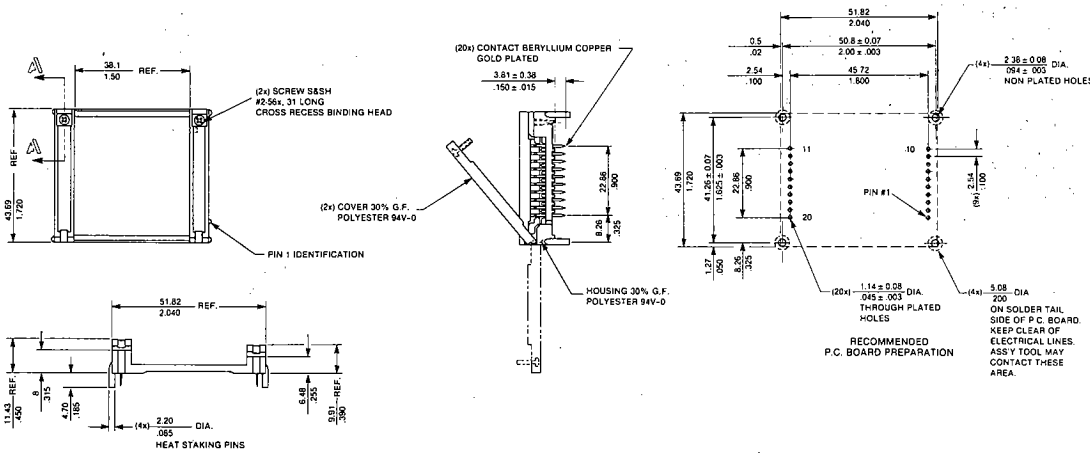
7110 PACKAGE SEATED IN SOCKET WITH ARMS UP



PACKAGE OUTLINE



MAJOR TRACK-MINOR LOOP ARCHITECTURE OF 7110 (ONE HALF SHOWN)



SOCKET OUTLINE

PIN DESCRIPTION

BOOT.REP (Pin 4)

Two-level current pulse input for reading the boot loop.

BOOT.SWAP (Pin 5)

Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM.

DET.COM (Pin 15)

Ground return for the detector bridge.

DET.OUT (Pins 16 through 19)

Differential pair (A+, A− and B+, B−) outputs which have signals of several millivolts peak amplitude.

DET.SUPPLY (Pin 20)

+12 volt supply pin.

GEN.A and GEN.B (Pins 7, 8)

Two-level current pulses for writing data onto the input track.

PULSE.COM (Pin 1)

+12 volt supply pin.

REP.A and REP.B (Pins 3 and 2)

Two-level current pulses for replicating data from storage loops to output track.

SWAP.A and SWAP.B (Pins 13, 14)

Single-level current pulse for swapping data from input track to storage loops.

X−.COIL.IN, X+.COIL.IN (Pins 9, 10)

Terminals for the X or inner coil.

Y−.COIL.IN, Y+.COIL.IN (Pins 11, 12)

Terminals for the Y or outer coil.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0–70°C
Relative Humidity	95%
Non-Volatile Storage Temperature	−40 to + 100°C
Shelf Storage Temperature (Data Integrity Not Guaranteed)	−65°C to +150°C
Voltage Applied to DET.SUPPLY or PULSE.COM	14 Volts
Continuous Current between PULSE.COM and Inputs	10 mA
Continuous Current between DET.COM and Detector Outputs	10 mA
Coil Current	0.5A D.C.
External Magnetic Field for Non-Volatile Storage	40 Oersteds
Non-Operating Handling Shock (without socket)	200G
Operating Vibration (2 kHz to 2 kHz with socket)	20G

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 25°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Nom.[1]	Max.		
R_1	Resistance: PULSE.COM to REP.A or REP.B		20		ohms	
R_2	Resistance: PULSE.COM to BOOT.REP		8		ohms	
R_3	Resistance: PULSE.COM to BOOT.SWAP		17		ohms	
R_4	Resistance: PULSE.COM to GEN.A or GEN.B		32		ohms	
R_5	Resistance: PULSE.COM to SWAP.A or SWAP.B		120		ohms	
R_6	Resistance: DET.COM to DET.OUT.A+ or DET.OUT.B+		640		ohms	
R_7	Resistance: DET.COM to DET.OUT.A– or DET.OUT.B–		670		ohms	
R_8	Resistance: DET.COM to DET.SUPPLY		510		ohms	
R_X	X Coil Resistance		5.2		ohms	
R_Y	Y Coil Resistance		2.7		ohms	
L_X	X Coil Inductance		98.5		μH	
L_Y	Y Coil Inductance		79		μH	

DRIVE REQUIREMENTS

T_A= Range specified in Table 1.

Symbol	Parameter	Min.	Nom.[1]	Max.	Units
f_R	Field Rotation Frequency	49.75	50.000	50.25	KHz
ϕ_L	Phase Lag from Y.COIL to X.COIL	85	90	95	Degrees
I_{PX}	X.COIL Peak Current		600		mA
I_{PY}	Y.COIL Peak Current		750		mA
T_{DX}	X.COIL Positive Turn On Phase		270		Degrees
T_{1X}	X.COIL Positive Turn On Width		108		Degrees
T_{2X}	X.COIL Positive Decay Width		72		Degrees
T_{3X}	X.COIL Negative Turn On Width		108		Degrees
T_{4X}	X.COIL Negative Decay Width		72		Degrees
T_{DY}	Y.COIL Positive Turn On Phase		0		Degrees
T_{1Y}	Y.COIL Positive Turn On Width		108		Degrees
T_{2Y}	Y.COIL Positive Decay Width		72		Degrees
T_{3Y}	Y.COIL Negative Turn On Width		108		Degrees
T_{4Y}	Y.COIL Negative Decay Width		72		Degrees
P_T	Total Coil Power		1.3		Watt

Note: 1. Nominal values are at T_A = 25°C.

CONTROL PULSE REQUIREMENTS

Nominal values at $T_A = 25°C$. See Notes 2 and 3.

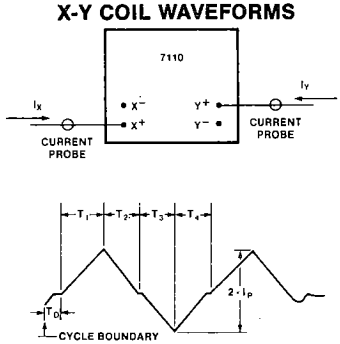
Pulse	Amplitude (mA)	Phase of Leading Edge (Degrees)	Width (Degrees)
GEN.A, GEN.B Cut	64	270 (Odd), 90 (Even)	4.5
GEN.A, GEN.B Transfer	36	270 (Odd), 90 (Even)	90
REP.A, REP.B Cut	180	270	4.5
REP.A, REP.B Transfer	140	270	90
SWAP	120	180	517
BOOT.REP Cut	90	270	4.5
BOOT.REP Transfer	70	270	90
BOOT.SWAP	70	180	See Note 4.

Note: 2. Pulse timing is given in terms of the phase relations as shown below. For example, a 7110 operating at $f_R = 50.000$ kHz would have a REP.A transfer width of 90° which is 5 μs.

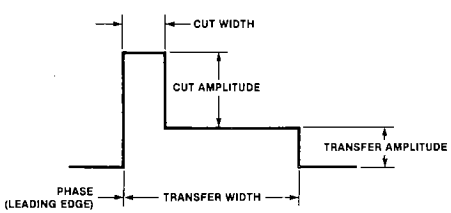
Table 1. 7110 Family

Part Number	T_A Range
7110	0-50°C
7110-1	0-70°C
7110-2	10-50°C
7110-3	10-35°C

X-Y COIL WAVEFORMS



3. Two level pulses are described as shown below.



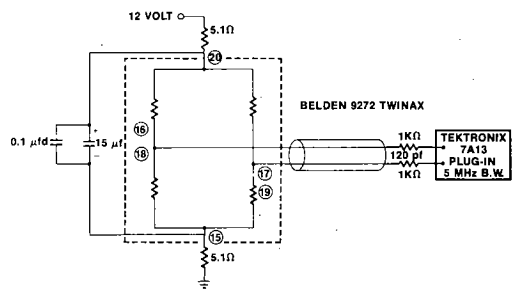
4. BOOT.SWAP is not normally accessed during operation. It is utilized at the factory to write the index address and redundant loop information into the bootstrap loops before shipment.

OUTPUT CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.

Symbol	Min.	Nom.	Max.	Units	Test Conditions
S_1		6		mV	See Figures below.
S_0		1		mV	

TEST SET-UP FOR OUTPUT VOLTAGE MEASUREMENT



DETECTOR OUTPUT WAVEFORMS